

Application No. 10/775,523
Amendment dated November 6, 2006
Reply to Final Office Action of September 6, 2006

Amendments To the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 Claim 1 (currently amended): A switch coupled between a plurality of host units and a
2 device for routing frame information therebetween and comprising:
3 a. a first serial advanced technology attachment (ATA) port including a first host task
4 file, capable of receiving] responsive to a non-data frame information structure
5 (FIS) and coupled to a first host unit;
6 b. a second serial ATA port including a second host task file, [capable of receiving]
7 responsive to a non-data FIS,] and coupled to a second host unit;
8 c. a third serial ATA port, [capable of receiving] responsive to a non-data FIS, and
9 coupled to a device; and
10 d. an arbitration and control circuit for selecting one of the first host or second host
11 units to concurrently access the device, through the switch, by accepting
12 [commands] non-data FIS, from either of the first or second host units, at any
13 given time, including when the device is not in an idle state and whenever either
14 one of the first or second host units sends non-data FIS to the device and further
15 wherein the non-data FIS of the first and second host units and the device identify
16 which one of the first or second host units is an origin and/or destination host so
17 that routing of non-data FIS is transparent to the switch thereby reducing the
18 complexity of the design of the switch rendering its manufacturing less expensive.

1 Claim 2 (original): A switch as recited in claim 1 wherein said device is a storage unit.

1 Claim 3 (original): A switch as recited in claim 1 wherein said switch is employed in an
2 enterprise system.

1 Claim 4 (original): A switch as recited in claim 1 wherein said arbitration and control circuit
2 causes concurrent access of the device by the first and second host units.

1 Claim 5 (currently amended): A switch as recited in claim 1 wherein a bit is used to indicate
2 which host is the origin or destination of the non-data FIS.

1 Claim 6 (original): A switch as recited in claim 1 wherein said first, second and third ports
2 are layer 2 ports.

1 Claim 7 (original): A switch as recited in claim 1 wherein the switch provides for 'route
2 aware' routing.

1 Claim 8 (currently amended): A switch as recited in claim 1 wherein the switch [switches
2 between layer 2 and] further includes a dual ported first-in-first-out (FIFO).

1 Claim 9 (currently amended): A switch comprising:
2 a. a first serial advanced technology attachment (ATA) port including a first host
3 task file, [capable of receiving] responsive to a non-data frame information
4 structure (FIS)[,] and for connection to a first host unit;
5 b. a second serial ATA port including a second host task file[, capable of
6 receiving] responsive to a non-data FIS, for connection to a second host unit;
7 c. a third serial ATA port, [capable of receiving] responsive to a non-data FIS,
8 for connection to a device, the switch for routing frame information between
9 the first and second host units and the device; and
10 d. an arbitration and control circuit for selecting either the first host unit or the
11 second host unit to concurrently access the device, through the switch, by
12 accepting [commands] non-data FIS, from either of the first or second host
13 units, at any given time, including when the device is not in an idle state, when
14 either one of the first or second host units sends non-data FIS to the device,
15 wherein while one of the first or second host units is coupled to the device, through
16 the switch, the other one of the first or second host units sends non-data FIS to the switch
17 for routing to the device and further wherein the non-data FIS of the first and second host
18 units and the device identify which one of the first or second host units is an origin and/or
19 destination host so that routing of non-data FIS is transparent to the switch thereby
20 reducing the complexity of the design of the switch rendering its manufacturing less
21 expensive.

1 Claim 10 (previously presented): A switch as recited in claim 9 wherein the switch provides
2 for 'route aware' routing.

1 Claim 11 (original): A switch as recited in claim 9 wherein said device is a storage unit.

1 Claim 12 (original): A switch as recited in claim 9 wherein said switch is employed in an
2 enterprise system.

1 Claim 13 (original): A switch as recited in claim [1] 9 wherein said arbitration and control
2 causes concurrent access of the device by the first and second host units.

1 Claim 14 (currently amended): A switch that is connectable to a first host unit, a second host
2 unit and a device via serial advanced technology attachment (ATA) links, for routing
3 frame information between the first and second host units and the device, said switch
4 comprising:

- 5 a. a first serial ATA port, [capable of receiving] responsive to a non-data frame
6 information structure (FIS), for connection to a first host unit;
- 7 b. a second serial ATA port, [capable of receiving] responsive to a non-data FIS,
8 for connection to a second host unit;
- 9 c. a third serial ATA port, [capable of receiving] responsive to a non-data FIS,
10 for connection to a device;
- 11 d. an arbitration and control circuit for selecting one of the first or second host
12 units to concurrently access the device through the switch, by accepting
13 [commands] non-data FIS, from either of the first or second host units, at any
14 given time, including when the device is not in an idle state, when either the
15 first or second host units sends non-data FIS to the device,
16 wherein while one of the first or second host units is coupled to the device, the
17 other one of to the first or second host units sends non-data FIS to the switch for
18 routing to the device and further wherein the non-data FIS of the first and second host
19 units and the device identify which one of the first or second host units is an origin
20 and/or destination host so that routing of non-data FIS is transparent to the switch
21 thereby reducing the complexity of the design of the switch rendering its
22 manufacturing less expensive.

1 Claim 15 (original): A switch as recited in claim 14 wherein the switch is a serial ATA
2 switch.

1 Claim 16 (original): A switch as recited in claim 14 wherein said device is a storage unit.

1 Claim 17 (original): A switch as recited in claim 14 wherein said switch is employed in an
2 enterprise system.

1 Claim 18 (original): A switch as recited in claim 14 wherein said arbitration and control
2 circuit causes concurrent access of the device by the first and second host units.

1 Claim 19 (currently amended): A method for communication between multiple host units
2 and a device, through a serial advanced technology attachment (ATA) switch coupled
3 to the multiple host units and the device using serial ATA links routing frame
4 information therebetween, comprising:
5

6 a. receiving a non-data frame information structure (FIS) through a first serial
7 ATA port, from a first host unit;
8 b. receiving a non-data FIS, through a second serial ATA port, from a second
9 host unit;
10 c. receiving a non-data FIS through a third serial ATA port;
11 d. arbitrating between the first and second host units and the device;
12 e. selecting one of the first or second host units for coupling to the device
13 through the switch when either of the first or second host units sends
14 commands for execution by the device;
15 f. coupling the device to the selected one of the first or second host units; and
16 g. while the selected one of the first or second host units is coupled to the device,
17 the other one of the first or second host units sending non-data FIS to the
18 switch for routing to the device
19 during the sending step g., the non-data FIS of the first and second host units and the
20 device identifying which one of the first or second host units is an origin and/or
21 destination host so that routing of non-data FIS is transparent to the switch thereby
22 reducing the complexity of the design of the switch rendering its manufacturing less
23 expensive.

1 Claim 20 (currently amended): A method for communication, as recited in claim 19,
2 further including the steps of transmitting a [frame information structure (FIS)] non-data

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- 3 FIS through the first serial ATA port, [transmitting a frame information structure (FIS)]
- 4 non-data FIS through the second serial ATA port, and transmitting a [frame information
- 5 structure (FIS)] non-data FIS through the third serial ATA port.